IN THE CLAIMS

Listing of Claims:

1   1. (currently amended) A method for managing power utilization and performance of a

2   multiprocessor (MP) system comprising the steps of:

3   receiving first sensor data defining physical parameters of said MP system;

4   receiving first parameters corresponding to customer level operational

5   requirements of said MP system;

6   determining power and performance goal settings for processors in said MP

7   system in response to said first sensor data and said first parameters;

8   generating a set of controls for said MP system in response to said power and

9   performance goal settings; and

10   applying said set of controls to adjust operation parameters of said processors in

11   said MP system.

1   2. (original) The method of claim 1, wherein said method further comprises the step of:

2   applying said controls to adjust operation parameters of cooling systems for said

3   MP system.

1   3. (original) The method of claim 1, wherein said MP system comprises a single

2   multiprocessor very large scale integrated circuit (VLSI) chip.

1   4. (original) The method of claim 3, wherein said MP system comprises a cooling

2   means for said multiprocessor VLSI chip.

1   5. (original) The method of claim 4, wherein said cooling means comprises a single chip

2   cooling fan.

1   6. (original) The method of claim 4, wherein said cooling means comprises a

2   controllable single chip thermo-electric cooler.

1 7. (original) The method of claim 3, wherein said MP system comprises a self-contained

2 MP system, said self-contained MP system comprising a plurality of said multiprocessor

3 VLSI chips, said self-contained MP system further comprising a first controllable cooling

4 system.

1 8. (original) The method of claim 7, wherein said MP system comprises a rack MP

2 system, said rack MP system comprising a plurality of said self-contained MP systems

3 and a controllable rack cooling system.

1 9. (original) The method of claim 8, wherein said MP system comprises a plurality of

2 said rack MP systems, said MP system further comprising a controllable MP system

3 cooling means.

1 10. (original) The method of claim 1, wherein said first sensor data comprises

2 temperatures of said processors in said MP system, supply voltages corresponding to

3 circuits in said processors, clock frequencies of said processors, electromagnetic radiation

4 (EMC) of said MP system, acoustic levels of said MP system, vibration levels of said MP

5 system, and air temperatures of cooling systems in said MP system.

1 11. (currently amended) The method of claim 1, wherein said first parameters comprise

2 customer level quality of service parameters for said MP system.

1 12. (original) The method of claim 1, wherein said first parameters comprise policy of

2 operation parameters for said MP system.

1 13. (original) The method of claim 11, wherein said quality of service parameters

2 comprise assignment data defining processor assignment to tasks performed by said MP

3 system, access availability data for processors in said MP system, performance level data

4 defining a performance for an application executing on processors of said MP system,

5 and processor operational data defining which of said processors are operational.

1   14. (original) The method of claim 12, wherein said policy of operation parameters
2   comprise data defining a cost of power for said MP system, acceptable acoustic noise
3   level data for said MP system, acceptable EMC output noise level data for said MP
4   system, acceptable output vibration level data of said MP system and acceptable
5   temperature level data for elements of said MP system.

1   15. (original) The method of claim 1, wherein said power and performance goals
2   comprise data defining a desired MP system power consumption level, data defining a
3   desired processor power consumption level, data defining desired MP system
4   temperatures, desired MP acoustic noise output levels, desired EMC noise levels, and
5   desired processor instruction execution speeds.

1   16. (original) The method of claim 1, wherein said set of controls comprise power
2   supply voltage settings for said processors, clock frequency settings for said processors,
3   cooling fan speeds, controls for said MP system cooling means and operational mode
4   settings for said processors.

1   17. (original) The method of claim 16, wherein said operational mode settings comprise
2   an active mode and a sleep low power mode.

1   18. (original) The method of claim 16, wherein said MP system cooling means
2   comprises channeled temperature conditioned air.

1   19. (currently amended) A controller for managing power and performance in a
2   multiprocessor MP system comprising:
3   a first receiving circuit operable to receive first sensor data corresponding to
4   physical parameters of said MP system;
5   a second receiving circuit operable to receive first parameters defining customer
6   level quality of service operational requirements of said MP system;

7   a third circuit operable to determine power and performance goal settings for said

8   processors in said MP system in response to said first data and said first parameters;

9   a fourth circuit operable to generate a set of controls for said MP system in

10   response to said power and performance goal settings; and

11   a fifth circuit operable to apply said set of controls to adjust operation parameters

12   of said processors in said MP system.

1   20. (original) The controller of claim 19, wherein said fifth circuit is further operable to

2   apply said set of controls to adjust operation parameters of cooling systems of said MP

3   system.

1   21. (original) The controller of claim 19, wherein said set of controls comprise power

2   supply voltage settings for said processors, clock frequency settings for said processors,

3   cooling fan speeds, controls for said MP system cooling means and operational mode

4   settings for said processors.

1   22. (original) The controller of claim 21, wherein said operational mode settings

2   comprise an active mode and a sleep low power mode.

1   23. (original) The controller of claim 21, wherein said MP system cooling means

2   comprises channeled temperature conditioned air, chilled fluid and solid state cooling

3   units.

1   24. (currently amended) A multiprocessor (MP) system comprising a plurality of

2   processors and a controller for managing power and performance in said MP system, said

3   controller further comprising:

4   circuitry for receiving first sensor data defining physical parameters of said MP

5   system;

6   circuitry for receiving first parameters corresponding to <u>customer level quality of</u>

7   <u>service</u> operational requirements of said MP system;

8   circuitry for determining power and performance goal settings for processors in

9   said MP system in response to said first sensor data and said first parameters;

10   circuitry for generating a set of controls for said MP system in response to said

11   power and performance goal settings; and

12   circuitry for applying said set of controls to adjust operation parameters of said

13   processors in said MP system.

1   25. (original) The MP system of claim 24, wherein said controller is one of said

2   plurality of processors in said MP system.

1   26. (original) The MP system of claim 24, further comprising:

2   circuitry for applying said controls to adjust operation parameters of cooling

3   systems for said MP system.

1   27. (original) The MP system of claim 24, wherein said MP system comprises a single

2   multiprocessor very large scale integrated circuit (VLSI) chip.

1   28. (original) The MP system of claim 27, wherein said MP system comprises a cooling

2   means for said multiprocessor VLSI chip.

1   29. (original) The MP system of claim 28, wherein said cooling means comprises a

2   single chip cooling fan.

1   30. (original) The MP system of claim 27, wherein said MP system comprises a self-

2   contained MP system, said self-contained MP system comprising a plurality of said

3   multiprocessor VLSI chips, said self-contained MP system further comprising a first

4   controllable cooling system.

1   31. (original) The MP system of claim 30, wherein said MP system comprises a rack MP

2   system, said rack MP system comprising a plurality of said self-contained MP systems

3   and a controllable rack cooling system.

1   32. (original) The MP system of claim 31, wherein said MP system comprises a plurality

2   of said rack MP systems, said MP system further comprising a controllable MP system

3   cooling means.

1   33. (original) The MP system of claim 24, wherein said first parameters comprise policy

2   of operation parameters for said MP system.